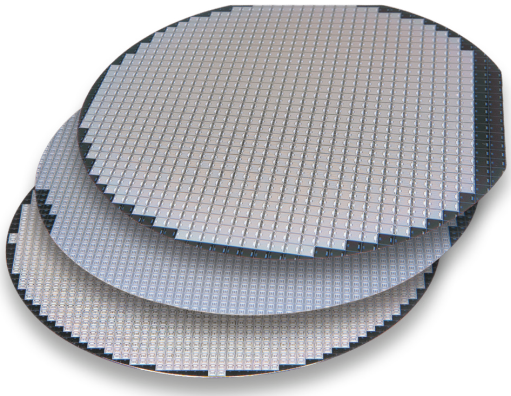
Standard bare die devices

A Legacy of Innovation

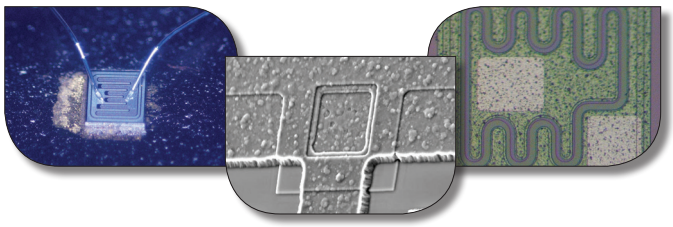
Central Semiconductor Corp. has been in the business of manufacturing discrete semiconductors since 1974.

In 1996, Central entered the hybrid market to fill the void left after the departure of several manufacturers from the bare die market. This guide features Central's standard processes available in bare die. Full wafer or chip tray packing options are available.



Bare die devices:

- Diodes
- Rectifiers
- Transistors
- TVS Diodes & ESD Protection Diodes
- MOSFETs/JFETs
- Thyristors



Devices available in:

- Fully probed wafers (rejects inked)
- Waffle tray packs (100% accepted die)
- Full wafer sawn on plastic ring (rejects inked)

Processes & facilities

- 100% of die is probed and rejects are inked
- All die are inspected in accordance to MIL-STD-750 Method 2073
- Probing performed in Central's Class 1000 clean room
- Majority of Central's die inventory is held in the U.S. at Hauppauge, NY facility

100% tested and screened in Central's Class 1000 clean room

Custom services & solutions

Your vision is our mission. Central excels at listening to customers' challenges and designing custom solutions that other manufacturers have no interest in pursuing. **Just ask.**

Solutions include the following:

- Electrical parameter screening
- Custom wafer diffusion and metallization
- Standard/customer-specific testing and up-screening

Up-screening capabilities

Central has the capability to perform up-screen testing in-house for high reliability applications.

MIL-PRF 38534
- Class H and K equivalents

MIL-PRF 19500
- Class HC and KC equivalents

Customer-specific up-screening
- Customer SCDs are reviewed and all requirements confirmed

Testing capabilities:

All tests performed to MIL-STD-750 or MIL-STD-883 (bare die) test methods.

Typical bare die up-screening process:

MIL-PRF-38534 Evaluation Elements

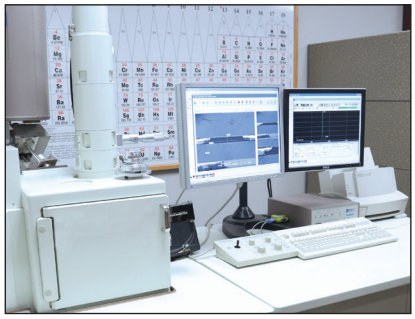
Sub Group	Class K	Class H	Test	MIL-STD-883 Method	MIL-STD-883 Conditions	Acceptance Quantity
1	X	X	Element electrical			100%
2	X	X	Visual inspection	2010 1/2069 1/2070 1/2072 1/2073		100%
3	X	X	Internal visual	2010 1/2069 1/2070 1/2072 1/2073		10 (0)
4	X		Temperature Cycling	1010	C	2/ 10 (0)
	X		Constant acceleration or mechanical shock	2002 - 2001	B, Y1 direction 3,000 g's, Y1 direction	
	X		Internal electrical			
	X		Burn in	1015	240 hours minimum at +125°C	
	X		Post burn in electrical			
	X		Steady state life	1005		
	X	X	Final electrical			
5	X	X	Wire bond evaluation	2011		10 (0) wires or 20 (1) wires
6	X		SEM	2018 1/2077		See method 2018 of MIL-STD-883 or method 2077 of MIL-STD-750

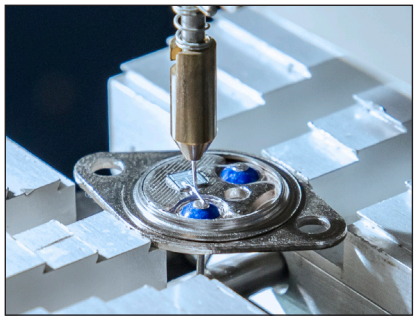
1/ MIL-STD-750 methods.

2/ For Class K sample sizes, see MIL-PRF-38534 Section C.3.3.4.1.

Thermal cycle testing


Temperature cycle chambers


Scanning Electron Micropsy (S.E.M.)


Wire pull testing